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EXAMINER	
HSU, JONI	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/726,220	FOULADI ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,16-23,25,27-35,37,39,40,43-51,53 and 54* is/are rejected.

7)☒ Claim(s) *13,15,24,26,36,38,41,42 and 52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 14, 2008 has been entered.

Response to Arguments

2. Applicant's arguments filed January 14, 2008 are considered but are not persuasive.

3. As per Claim 1, Applicant argues various claims define what is meant by memory controller and Examiner's attempts to compare prior art to example embodiments disclosed in specification and to limit claims to these example embodiments are legally improper (p. 12).

Examiner points out Examiner is not attempting to limit claims to example embodiments, but in fact is giving claims their broadest reasonable interpretation in light of supporting disclosure (MPEP 2106 II C). By stating that Chin (US006202101B1) reads on claims in light of example embodiments, Examiner is stating that claims can be broadly interpreted in light of example embodiments in such a manner that device of Chin reads on claims.

4. Applicant argues examples in Applicant's disclosure show memory interface/controller 152 as being separate from processor interface 150 and peripheral controller 162. Applicant's disclosure does not use term "memory controller" to collectively refer to processor interface 150, memory interface/controller 152, and peripheral controller 162. Applicant's disclosure supports

Applicant's position that Examiner improperly uses "memory controller" to collectively refer to separate PCI, processor and memory controllers in Chin (US006202101B1) (p. 13).

Examiner points out Fig. 8 of Applicant's drawings shows diagram of memory controller (p. 10, ll. 5), and shows memory controller comprises interfaces including queues and arbitration control 825 (p. 26, ll. 7-9, 25; p. 27, ll. 1-11). Fig. 2 of Chin shows diagram of bus interface unit 14, and shows that bus interface unit 14 comprises queues 50 and memory controller 44. Comparing Fig. 2 of Chin with Fig. 8 of Applicant's drawings, it seems that memory controller 44 of Chin by itself should not be considered to be equivalent to entire memory controller shown in Fig. 8 of Applicant's drawings, since memory controller 44 of Chin by itself does not contain queues that are shown to be part of memory controller of present invention. Memory controller 44 of Chin performs arbitration (c. 8, ll. 56-62), and so is considered to be equivalent to arbitration control 825 of present invention. Claim 1 recites "…memory controller comprising…", so this is taken to mean memory controller must contain all limitations recited, but, it is not limited to only the limitations recited. So, claims do not expressly recite memory controller cannot be combined in common unit along with other interface controllers and memory controller must be separate entity from all other interface controllers.

5. Applicant argues while Chin describes passing cycles between controllers using queues, there is no basis for Examiner's contention that cycles passed using queue 50c are memory cycles. Chin describes queue 50c is "memory-to-processor" queue. Queues 50d and 50h store data read from memory, not requests for such data (p. 13).

In reply, Chin teaches multiple resource buffer 68 receives memory requests from processor bus (c. 12, ll. 44-47). Memory request will access memory location and data at that

location is temporarily stored within M2P queue 50c (c. 12, ll. 65-67). M2P queue 50c is connected between memory 18 and processor 12, and so M2P queue 50c is connected to processor bus. M2I queue 50d and M2A queue 50h work in similar manner as M2P queue 50c, except they are for PCI and AGP respectively instead of processor (c. 8, ll. 33, 36; c. 9, ll. 20-35). So, 50c, 50d, and 50h are considered to be buffer memories, each buffer memory being operatively coupled to one of resources requesting access to main memory for storing information indicative of request for main memory access, as recited in Claim 1.

6. As per Claim 14, Applicant argues Chin teaches de-queuing for queue 50c, which contains data whose source is memory and whose destination is processor. This queue is not write request queue and Chin does not teach initiating flushing of resource's write request queue when resource is writing to main memory (p. 14). As per Claim 40, cited passage simply describes how long address is held in queue. There is no flushing of write request queue (p. 16).

In reply, Examiner points out Chin describes, "Arranging the order in which data is de-queued from queue 50c depends on where the pointer is relative to queue 64. For example, if pointer 76 is at entry numeral 0, then data is not de-queued from queue 50c until pointer arrives at entry number 1, in the example shown. Once pointer 76 is at entry number 1, then data attributed to entry numeral 1 is de-queued and thereafter presented to the processor bus. If the memory request is a write request, then the address will be held in P2M queue (queue 50a) until that request's entry number matches the current in-order queue entry number" (c. 13, ll. 1-11). Since this describes how long address is held in queue, it also teaches address will eventually not be held in queue any longer, and so will be de-queued. So, for case of write request queue, once request's entry number matches current in-order queue entry number, then data attributed to

entry number is de-queued. So, Chin does disclose initiating flushing of resource's write request queue when resource is writing to main memory.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-7, 14, 16-18, 25, 27-30, 37, 39, 40, 43-46, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) in view of Harriman (US006092158A).

10. As per Claim 1, Chin teaches in graphics system including main processor (12, Fig. 1) and graphics processing system (20) for generating graphics images on display in cooperation with main processor (c. 1, ll. 56-59; *CPU bus connects a CPU 12 to a bus interface unit 14, interface unit 14 may also include a graphics port to allow communication to a graphics accelerator 20*, c. 7, ll. 21-37), and main memory (18), system including plurality of resources (40, 42, 46, Fig. 2) requesting access to main memory, memory controller comprising plurality

of buffer memories (50a, 50c, 50e, 50d, 50g, 50j, Fig. 2), each of buffer memories being operatively coupled to one of plurality of resources requesting access to main memory for storing information indicative of request for main memory access (c. 8, ll. 20-37). Memory controller 44 in Chin (*memory controller 44 arbitrates*, c. 8, ll. 56-62) is considered to be equivalent to arbitration control (825, Fig. 8) of present invention. Interface controller 14 in Chin (*bus interface unit provides an interface between components clocked at similar rates, bus interface unit 14 contains a memory controller*, c. 7, ll. 27-31) is considered to be equivalent to memory controller (Fig. 8) of present invention. So, queues in Chin are part of memory controller. Chin discloses multiple resource buffer memory (memory request queue 68, Fig. 6) coupled to plurality of buffer memories for storing requests for main memory access from each of plurality of resources; and control circuit for controlling transfer of information from plurality of buffer memories to multiple resource buffer memory (*temporarily stored within a M2P queue 50c*, c. 12, ll. 65-67; *type stored in the output pointer location within the in-order queue determines if the data at the head output pointer location is either read or write data, and thus whether the data is to be drawn from or sent to M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64*, c. 13, ll. 51-c. 14, ll. 5). Chin teaches processor controller 42 is part of interface controller 14 (c. 8, ll. 23-26), which is equivalent to memory controller. So, queue 68 is part of memory controller. Chin teaches memory request queue 68 is coupled to plurality of buffer memories (queues) for storing requests for main memory access from each of plurality of resources (processors) (*temporarily stored within a M2P queue 50c*, c. 12, ll. 65-67; *type stored in the output pointer location within the in-order queue determines if the data at the head output*

pointer location is either read or write data, and thus whether the data is to be drawn from or sent to M2P or P2M (attributed to memory data queue), the memory request queue entry numbers are used to resolve snoop results maintained in the in-order queue 64, c. 13, ll. 51-c. 14, ll. 5), and so suggests control circuit involved in transferring information. Chin discloses memory request will access memory location and data at that location is temporarily stored within M2P queue 50c (c. 12, ll. 65-67). Type stored in output pointer location within in-order queue determines if data at head output pointer location is either read or write data, and thus whether data is to be drawn from or set to M2P or P2M (attributed to memory data queue). Memory request queue entry numbers are used to resolve snoop results maintained in in-order queue 64 (c. 13, ll. 51-c. 14, ll. 5). M2P queue 50c is buffer memory and memory request queue is multiple resource buffer. Since system has means for using in-order queue to control whether data is to be drawn from M2P queue and memory request queue snoops results maintained in in-order queue, this means there is means for controlling transfer of information from M2P queue 50c (buffer memory) to memory request queue (multiple resource buffer), and so Queue 50c is related to this concept. Since memory request will access memory location and data at that location is temporarily stored within a M2P queue 50c (c. 12, ll. 65-67), and there are plurality of these queues (c. 8, ll. 30-37), Chin discloses plurality of queues (buffers) each of which is operatively coupled to one of plurality of resources (processors) requesting memory access.

However, Chin does not disclose means to reduce frequency of switching from main memory write operations to main memory read operations. However, Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*,

c. 1, ll. 35-50) similar to instant claim limitation "to reduce the frequency of switching from main memory write operations to main memory read operations".

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Chin to include means to reduce frequency of switching from main memory write operations to main memory read operations as suggested by Harriman because it results in improved and optimized overall memory access performance.

11. As per Claim 2, Chin discloses plurality of buffer memories (50a, 50e, 50g, Fig. 2) are main memory write queues (c. 8, ll. 20-37).

12. As per Claim 3, Chin discloses multiple resource buffer memory (68, Fig. 4) is main memory write queue (c. 11, ll. 9-20).

13. As per Claim 4, Chin discloses plurality of buffer memories (50a, 50e, 50g, Fig. 2) are main memory write queues (c. 8, ll. 20-37), and wherein multiple resource buffer memory (68, Fig. 6) is main memory write queue (c. 11, ll. 9-20), and wherein control circuit (44, Fig. 2) is operable to control rate at which write requests are coupled to multiple resource buffer memory from plurality of buffer memories (*Memory controller 44 arbitrates among processor write, processor reads, peripheral writes, peripheral reads and refresh. Arbitration for each cycle is pipelined into the current memory cycle which ensures that the next memory address is available on the memory bus before the current cycle is complete*, c. 8, ll. 52-67; c. 13, ll. 51-c. 14, ll. 5).

14. As per Claim 5, Chin discloses plurality of buffer memories (50a, 50e, 50g, Fig. 2) are main memory write queues and further including plurality of main memory read queues (50c, 50d, 50j), each read queue being operatively coupled to resource (40, 42, 46) requesting to read information from main memory (18, Fig. 1) (c. 8, ll. 20-37).

15. As per Claim 6, Chin teaches control circuit (44, Fig. 2) includes arbitration circuitry for arbitrating requests for access to main memory (18, Fig. 1) (c. 8, ll. 56-62).

16. As per Claims 7, 18, 30, and 46, Chin teaches arbitration circuitry is operable to control frequency with which requesting resources are enabled to participate in arbitrating for main memory access (c. 8, ll. 56-67).

17. As per Claims 14, 25, and 37, Chin teaches plurality of buffer memories (50a, 50c, 50e, 50d, 50h, 50g, 50j, Fig. 2) and multiple resource buffer memory (68, Fig. 5) are write request queues (c. 8, ll. 20-37; c. 11, ll. 9-20), and resource that is writing to main memory generates flush signal for initiating flushing of that resource's write request queue (de-queuing, c. 13, ll. 1-11). Chin discloses memory request will access memory location and data at that location is temporarily stored within an M2P queue 50c (c. 12, ll. 65-67), and so queue 50c is write request queue. Chin discloses de-queuing operation for queue 50c (c. 13, ll. 1-11), and so Chin discloses initiating flushing of resource's write request queue when resource is writing to main memory.

18. As per Claim 16, Chin discloses in information processing system including main processor (12, Fig. 1; 42, Fig. 2), main memory (18, Fig. 1), and at least first (40, Fig. 2) and second resource (46) competing with main processor for access to main memory (c. 1, ll. 56-59; c. 7, ll. 21-37; c. 8, ll. 20-37), memory controller (14) comprising main processor related interface including main processor read request queue (50c) and main processor write request queue (50a); first resource related interface including at least one of first resource read request queue (50d) and first resource write request queue (50e); second resource related interface including at least one of second resource read request queue (50h) and second resource write request queue (50g) (c. 8, ll. 20-37); multiple resource write request queue (memory request

queue 68, Fig. 6) for receiving requests for writing to main memory; and memory access control circuit for granting access to main memory, memory access control circuit being coupled to receive read requests from each of read request queues and for receiving write requests from multiple resource write request queue (c. 12, ll. 65-67; c. 13, ll. 51-c. 14, ll. 5).

19. As per Claim 17, it is similar in scope to Claim 1, and so is rejected under same rationale.

20. As per Claims 27 and 43, Chin discloses in information system including main processor (12, Fig. 1), main memory (18), and at least first (40, Fig. 2) and second resource (46) competing with main processor for access to main memory (c. 1, ll. 56-59; c. 7, ll. 21-37; c. 8, ll. 20-37), method of controlling access to main memory comprising steps of storing requests for main memory access from first resource in first resource request queue (50d, 50e); storing requests for main memory access from second resource in second resource requests queue (50h, 50g) (c. 8, ll. 20-37); and granting requests for main memory access by memory access control circuit (c. 12, ll. 65-67; c. 13, ll. 51-c. 14, ll. 5).

However, Chin does not teach delaying forwarding requests for main memory access to memory access control circuit to reduce frequency of switching between memory read states and memory write states. However, Harriman discloses separation of read and write access to optimize overall memory access times by grouping reads and writes to reduce bus turn around (*grouping reads and writes may also reduce "turn around"*, c. 1, ll. 35-50) similar to instant claim limitation "delaying forwarding requests for main memory access to a memory access control circuit to reduce the frequency of switching between memory read states and memory write states". This would be obvious for reasons for Claim 1.

21. As per Claim 28, Chin teaches storing requests in multiple resource write queue (68, Fig. 4; c. 11, ll. 9-20).

22. As per Claim 29, it is similar in scope to Claim 28, so is rejected under same rationale.

23. As per Claims 39 and 53, Chin discloses step of granting requests includes step of fulfilling requests for main memory access in order requested (*maintains prior ordering of data sent to and returned from the memory*, c. 1, ll. 9-15).

24. As per Claim 40, Chin discloses in information system including main processor (12, Fig. 1), main memory (18), and at least first (40, Fig. 2) and second resource (46) competing with main processor for access to main memory (c. 1, ll. 56-59; c. 7, ll. 21-37; c. 8, ll. 20-37), method of controlling access to main memory comprising steps of storing requests for writing to main memory from first resource in first resource write request queue (50d, 50e); writing to main memory by first resource (c. 8, ll. 20-37); generating write queue flush signal by first resource to initiate copying information in first resource write request queue to main memory; and flushing first resource write request queue (de-queuing, c. 13, ll. 1-11).

25. As per Claims 44, 45, and 54, these claims are similar in scope to Claims 28, 29, and 1 respectively and therefore are rejected under the same rationale.

26. Claims 8-12, 19-23, 31-35, and 47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin (US006202101B1) and Harriman (US006092158A) in view of Jeddeloh (US006330647B1).

27. As per Claims 8, 19, 31, 47, Chin and Harriman are relied on for teachings for Claim 1.

However, Chin and Harriman do not teach memory access control register associated with one of resources, wherein control circuit includes arbitration circuitry responsive to contents

of memory access control register for determining frequency that resource is permitted to participate in arbitrating for main memory access. However, Jeddeloh discloses arbiter 210 in combination with configuration registers 214 to record access count values for each requestor (resources or class of requester) and counters 214 may be used by arbiter 210 to track number of memory access operations remaining for selected requester (c. 3, ll. 53-67; c. 4, ll. 1-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Chin and Harriman to include memory access control register associated with one of resources, wherein control circuit includes arbitration circuitry responsive to contents of the memory access control register for determining frequency that resource is permitted to participate in arbitrating for main memory access as suggested by Jeddeloh because it provides for efficient memory access control without denying access to those requestors issuing single access transactions and/or low priority requests for unacceptable long time (c. 1, ll. 48-51).

28. As per Claims 9, 20, 32, and 48, Chin does not teach set of control registers, control registers being programmable by main processor. But, Jeddeloh teaches control registers (configuration registers 212) being programmable by main processor (system controller 102) (*system controller 102 may set and adjust requestor access count values (i.e., modify values stored in configuration register 212*, c. 5, ll. 1-10). This is obvious for reasons for Claim 8.

29. As per Claims 10, 21, 33, and 49, Chin discloses control circuitry (44, Fig. 2) is operable to arbitrate between the resources for granting requests for main memory access (c. 8, ll. 56-62).

However, Chin does not teach control registers include plurality of memory bandwidth control registers which are accessed by control circuitry in determining which resource will be granted main memory access. However, Jeddeloh discloses this implicitly (*count values may be*

determined dynamically at...system start up and/or modified during system operations...access count values may be based on requestor operating speed, wherein faster devices are allocated larger access count values, c. 5, ll. 1-10). This would be obvious for reasons for Claim 8.

30. As per Claims 11, 22, 34, and 50, Chin does not teach each of memory bandwidth control registers is respectively associated with resource seeking main memory access. However, Jeddeloh discloses wherein each of memory bandwidth control registers (configuration registers 212) is respectively associated with resource seeking main memory access (*configuration registers 212 may be used to record access count values for each requestor (or class of requestor)*, c. 4, ll. 1-6). This would be obvious for reasons for Claim 8.

31. As per Claims 12, 23, 35, and 51, Chin does not teach control registers include at least one register associated with main memory access requesting resource for storing data for requesting resource indicative of at least one of memory usage and memory bandwidth for that resource. However, Jeddeloh discloses implicitly at least one register for requesting resource indicative of at least one of memory usage and memory bandwidth for that resource (*configuration registers 212 may be used to record access count values...counters 214 may be used by arbiter 210 to track number of memory access operations*, c. 4, ll. 1-6). This would be obvious for reasons for Claim 8.

Allowable Subject Matter

32. Claims 13, 24, 36, and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art fails to particularly disclose a register indicative of wasted memory cycles due to granting memory access to that resource.

33. Claims 15, 26, 38, 41, and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628